AMENDMENTS TO THE DRAWINGS

Figures 1 and 3 have been amended. New Figure 1A has been added. The attached sheets of formal drawings replace the original sheets including Figures 1 and 3.

REMARKS/ARGUMENTS

Claims 1, 2, and 4-13 were pending in this application. According to the July 29, 2005 Office Action, claims 1, 2, 4, 5, and 9-13 were rejected, claims 6-8 were allowed, and the drawings were objected to. Applicants have amended claims 1, 9, and 13 and have canceled claim 5. Accordingly, claims 1, 2, 4, and 6-13 are under consideration. Applicants have also amended the specification, amended Figures 1 and 3, and added new Figure 1A. Applicants maintain that the amendments do not introduce any new matter.

Allowed Subject Matter

Applicants note with appreciation that the Examiner has indicated that claims 6-8 are allowed.

Amended and New Drawings

In paragraph 1 of the Office Action, the Examiner objected to Figure 1, indicating that several nodes are missing as shown in Exhibit B of the Office Action. In response thereto, applicants have amended Figure 1 to add the indicated nodes. Applicants have also amended Figure 3 to add the labels "MP2" and "MP3" to two of the switches for consistency with paragraph [0029] of the specification. Applicants are submitting with this Response replacement Figures for Figures 1 and 3 reflecting the above changes and respectfully request that the replacement Figures be entered.

In paragraph 2 of the Office Action, the Examiner suggested that a simplified circuit schematic of Figure 1 be added to the application and in particular, suggested a circuit schematic similar to that shown in Exhibit A of the Office Action. In response to the Examiner's suggestion, applicants are submitting with this Response new Figure 1A and respectfully request that the new Figure be entered.

In accordance with new Figure 1A, applicants have amended the specification to add new paragraph [0010.1], which describes Figure 1A, and to amend paragraphs [0018], [0025], [0026], and [0028] to make reference to Figure 1A.

Rejection of Claims 1, 2, 4, 5, and 9-12 in view of Chee et al.

The Examiner rejected previously presented claims 1, 2, 4, 5, and 9-12 as unpatentable, 35 U.S.C. 102(a), in view of Chee et al., patent 6,369,665, April 9, 2002 (hereinafter Chee). In response thereto, applicants have amended independent claims 1 and 9 and canceled claim 5. Beginning with amended claim 1, it now recites an integrated circuit with an oscillator, comprising:

> a switch control . . . ; a plurality of current sources switchably connected to the timing element and for providing a second timing rate for the timing element, the second timing rate and a first timing rate determining an oscillation period of the oscillator; a switching circuit . . . being operable to select which of the plurality of current sources is connected to the timing element to provide the second timing rate; and wherein the output of the switch control causes the switching circuit to connect the selected current source to the timing element during each oscillation period.

Contrary to amended claim 1, Chee teaches an oscillator where the current sources are combined to provide a single timing rate, rather than a first and a second timing rate. In addition, Chee does not teach an oscillator "wherein the output of the switch control causes the switching circuit to connect the selected current source to the timing element during each oscillation period." Rather, Chee teaches that the combined current sources are connected and thereafter remain connected to the timing element.

Specifically, as shown in Chee Figure 5, Chee teaches an oscillator that operates in either a free-running mode or a synchronized clock mode. In the free-running mode, up/down counter 510 initially loads a preset value that causes one or more of current sources 520 to combine with current source 550. These combined current sources 550 and 520 thereafter charge capacitor 110 at a single timing rate that determines the frequency (or period) of the oscillator. (Chee, column 5, lines 15-28). Contrary to amended claim 1, current sources 550 and 520 do not charge the capacitor 110 at a second timing rate such that "the second timing rate and a first timing rate [determine] an oscillation period of the oscillator."

In addition, when the oscillator is in the free-running mode, the output of comparators 560/570 (which the Examiner equated to the switch control of claim 1) does not cause logic 580

and up/down counter 510 (which the Examiner equated to the switching circuit of claim 1) "to connect the selected current source to the timing element," contrary to claim 1. Up/down counter 510 connects the current sources to capacitor 110 independently of comparators 560/570 and comparators 560/570 only operate during each oscillation period to cause latch 140 to discharge capacitor 110.

As for the synchronized clock mode, Chee teaches that an external clock is now connected to the oscillator of Figure 5, thereby causing the oscillator to synchronize to the clock frequency. Here, Chee further teaches that the oscillator adjusts such that a pre-selected peak voltage at capacitor 110 remains constant regardless of the clock frequency. Specifically, when in synchronized clock mode, the external clock and one shot 540 now operate to cause latch 140 to discharge capacitor 110, thereby synchronizing the operating frequency of the oscillator to the clock. However, when the clock is initially interfaced to the oscillator, depending on whether the clock is operating at a higher or lower frequency than the previous operating frequency of the oscillator, the capacitor may not sufficiently charge to the pre-selected peak voltage or may over charge beyond the peak voltage. Here, the oscillator operates to return the capacitor to the peak voltage. For example, assuming the clock causes the oscillator to operate at an increased frequency, capacitor 110 will initially not charge to the peak voltage before being caused to discharge. Here, comparators 560/570 cause up/down counter 510 to combine one or more of current sources 520 with current source 550 until the combined current sources charge capacitor 110 at a sufficient rate to reach the peak voltage before the capacitor is caused to discharge. Once the capacitor is again charging to the peak voltage, comparators 560/570 cause up/down counter 510 to stop combining additional current sources with current source 550, the resulting combination of current sources thereafter charging the capacitor at a single timing rate during each oscillation period. (Chee, column 5, lines 29-62).

Contrary to amended claim 1, when the oscillator is in the synchronized clock mode, current sources 550 and 520 do not charge the capacitor 110 at a "second timing rate and a first timing rate [that determine] an oscillation period of the oscillator." The external clock determines the oscillation period of the oscillator and the current sources operate together to charge the capacitor at a single rate during the oscillation period. In addition, while Chee teaches

that the output of comparators 560/570 operate to cause logic 580 and up/down counter 510 to connect additional current sources to the capacitor 110, Chee does not teach that the output of comparators 560/570 cause logic 580 and up/down counter 510 "to connect the selected current source to the timing element during each oscillation period," contrary to claim 1. Once the combined current sources are sufficiently charging capacitor 110 to the peak voltage, comparators 560/570 only cause up/down counter 510 to maintain the resulting combination of current sources, not to connect the selected current sources to the capacitor during each oscillation period.

Accordingly, for the foregoing reasons, Chee fails to teach amended claim1, in addition to claims 2 and 4, which depend therefrom.

Turning to amended claim 9, it now recites a circuit for providing a plurality of oscillator output values, comprising:

> a timing component . . . ; a plurality of timing sources switchably connected to the timing component to provide a second timing interval for the timing component, the second timing interval and a first timing interval determining an oscillation period of the output value; a switch for selecting which of the plurality of timing sources to connect to the timing element to provide the second timing interval; and a switch control for controlling when during each oscillation period the switch connects the selected timing sources to the timing element to provide the second timing interval.

Contrary to amended claim 9, Chee does not teach that current sources 550 and 520 "provide a second timing interval for the timing component, the second timing interval and a first timing interval determining an oscillation period of the output value." As described above, for the free-running mode, Chee teaches that current sources 550 and 520 operate together to provide a single timing interval for capacitor 110 that determines the oscillation period . For the synchronized clock mode, Chee teaches that the external clock determines the oscillation period and that the current sources provide a single timing interval during the oscillation period.

In addition, Chee does not teach that comparators 560/570 control "when during each oscillation period [logic 580 and up/down counter 510 connect] the selected timing sources to the timing element to provide the second timing interval." As indicated above, in the free-running

mode, up/down counter 510 connects the current sources to capacitor 110 independently of comparators 560/570 and comparators 560/570 only operate during each oscillation period to cause latch 140 to discharge capacitor 110. In the synchronized clock mode, once the combined current sources are sufficiently charging capacitor 110 to the peak voltage, comparators 560/570 cause up/down counter 510 to maintain the resulting combination of current sources, not to connect the selected current sources to the capacitor during each oscillation period to provide a second timing interval. As such, Chee does not teach amended claim 9, or claims 10-12, which depend therefrom.

Rejection of Claims 9, 11, and 12 in view of Nicolai

The Examiner rejected previously presented claims 9, 11, and 12 as unpatentable, 35 U.S.C. 102(b), in view of Nicolai., patent 5,070,311, December 3, 1991 (hereinafter Nicolai). Referring to Nicolai Figure 1, Nicolai teaches an oscillator where register R1 is loaded with a value that causes one or more of current sources I - 2^nI to combine with current source I_0. These combined current sources act together to provide a single charging current (i.e., timing interval) that charges capacitor C at a single charging rate that determines the frequency of the oscillator. (Nicolai, column 4, line 63 to column 5, line 45).

Contrary to amended claim 9, Nicolai does not teach that current sources I_0 and I - 2^nI (which the Examiner equated to the timing sources of claim 9) "provide a second timing interval" for capacitor C or that a "second timing interval and a first timing interval [determine] an oscillation period of the output value" of the oscillator. Nicolai only teaches that current sources I_0 and I - 2^nI act together to provide a single timing interval for capacitor C to determine an oscillation period.

In addition, no where does Nicolai teach that register R1 (which the Examiner equated to the switch control of claim 9) controls "when during each oscillation period the switch connects the selected timing sources to the timing element to provide the second timing interval," contrary to amended claim 9. Nicolai only teaches that register R1 operates to initially configure which of the current sources I_0 and I - 2^nI are combined to provide a single timing interval for capacitor C and thereafter maintains that timing interval throughout each oscillation period.

Accordingly, Nicolai does not teach amended claim 9, or claims 11-12, which depend therefrom.

Rejection of Claim 13 in view of Gontowski

The Examiner rejected previously presented claim 13 as unpatentable, 35 U.S.C. 102(b), in view of Gontowski, patent 5,142,217, August 25, 1992 (hereinafter Gontowski). In response thereto, applicants have amended claim 13. Claim 13 now recites a circuit with an oscillator output, comprising:

> a plurality of current sources for providing a second slope, the second slope and a first slope forming portions of a waveform determining a period of the oscillator output; a switch for switching among the plurality of current sources to produce the second slope; a timing device output determined by the first slope; and a reference value for comparison with the timing device output to produce a control output, the control output being operable to influence the switch to select the second slope.

As shown in Figures 2 and 3, Gontowski teaches an oscillator where current source 14 produces an initial charging current that charges capacitor C_t at a first slope. Once capacitor C_t reaches a threshold voltage, comparator 20 enables a second current source 18 to combine with current source 14 to produce an increased charging current that charges capacitor C_t at a second slope. (Gontowski, column 6, line 50 to column 7, line 56). As shown in Figure 3, the two charging currents (i.e., the two slopes) determine a period of oscillation for the oscillator.

Significantly, contrary to amended claim 9, Gontowski does not teach or suggest a "plurality of current sources for providing a second slope" or a "switch for switching among the plurality of current sources to produce the second slope." Gontowski only teaches an oscillator with a single current source 18 for providing the second slope and a comparator 20 that is only capable of enabling this single current source. Accordingly, Gontowski fails to teach or suggest amended claim 13.

Conclusion

Since Chee, Nicolai, and Gontowski do not teach or suggest applicants' invention as now set forth in amended claims 1, 2, 4, and 9-13, applicants submit that these claims are clearly allowable. Favorable reconsideration and allowance of these claims are therefore requested.

Applicants earnestly believe that this application is now in condition to be passed to issue, and such action is also respectfully requested. However, if the Examiner deems it would in any way facilitate the prosecution of this application, he is invited to telephone applicants' counsel at the number given below.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450, on October 18, 2005:

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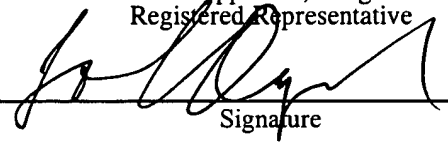

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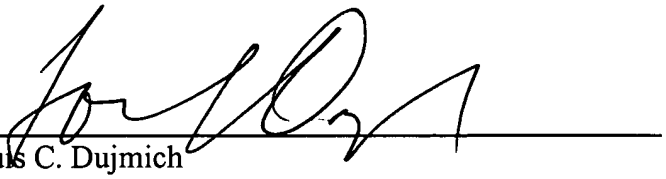
October 18, 2005
Date of Signature

Respectfully submitted,



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